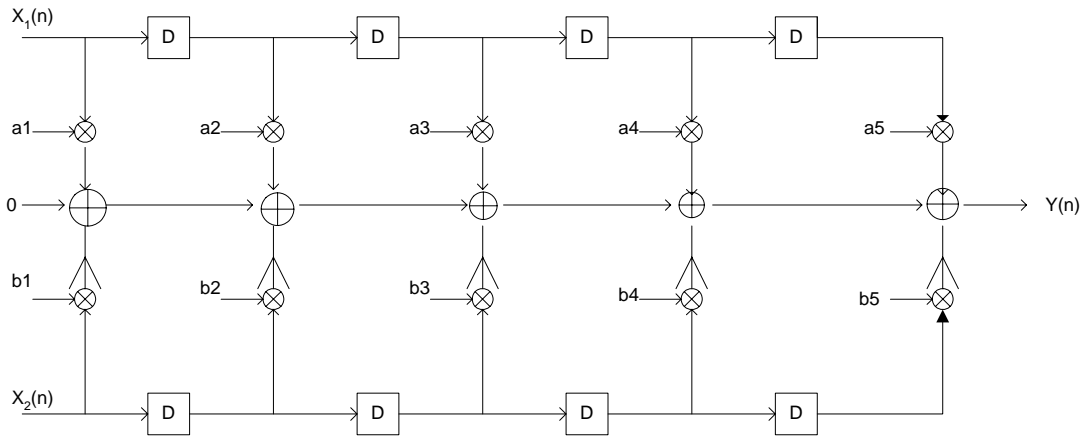


SOLUTIONS TO ASSIGNMENT NO.1

3. The given nonrecursive signal processing structure is shown as

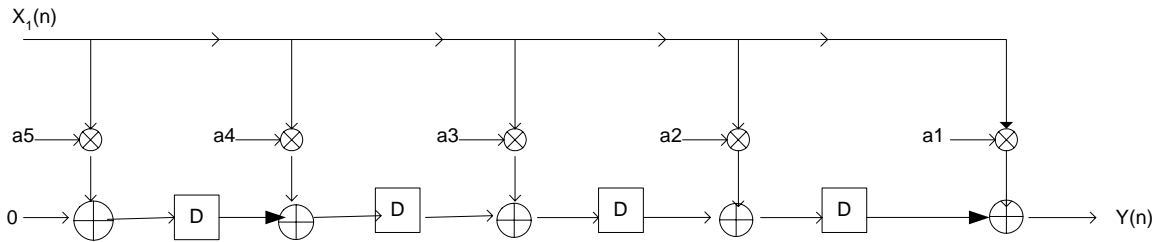


There are two critical paths, one from  $X_1(n)$  to  $Y(n)$  and the other from  $X_2(n)$  to  $Y(n)$ . The iteration along such a path is given by

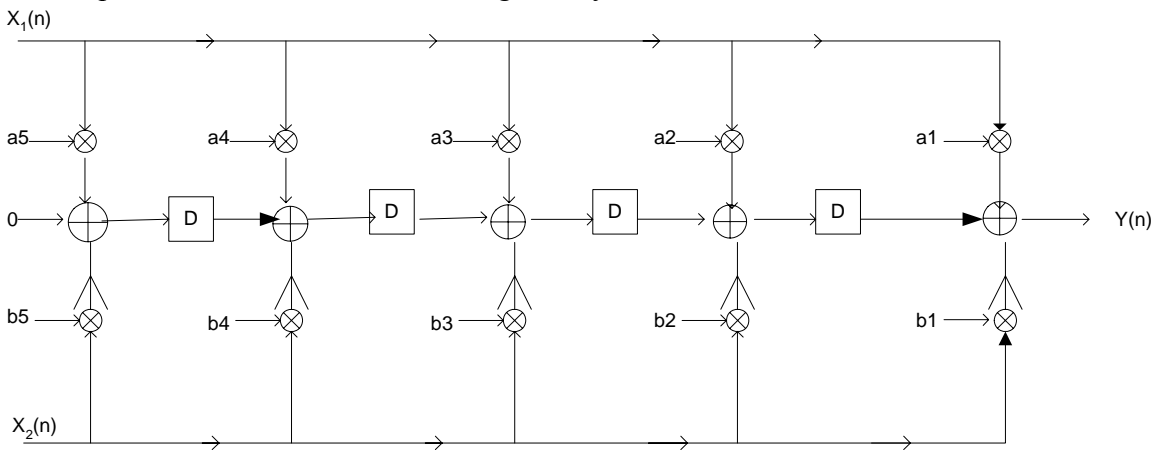
$$T_{\text{sample}} = T_m + 5 T_a$$

We can reduce this time period by dividing the whole circuit into two parts as below and using transposition on each part.

Transposing part 1 yields



Thus equivalent broadcast structure is given by



The iteration period for this broadcast circuit is

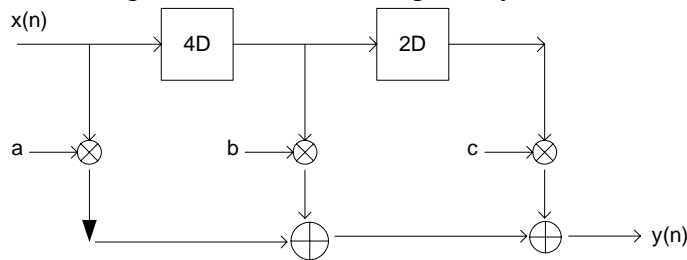
$$T_{\text{sample}} = T_m + T_a$$

Number of samples processed per second (throughput) is given by  $1 / (T_m + T_a)$ .

7. (a) The 6<sup>th</sup>-order FIR filter is given by

$$y(n) = ax(n) + bx(n-4) + cx(n-6)$$

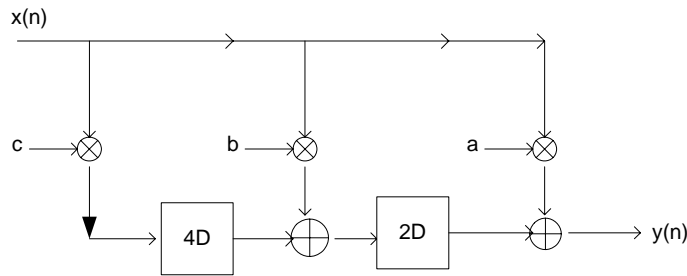
This circuit is represented in block diagram by



There are two critical paths from  $x(n)$  to  $y(n)$ . The iteration along critical path is given by

$$T_{\text{sample}} = T_m + 2 T_a$$

To limit the clock period by one multiply-add time we use transposition on the circuit above and get the new circuit as



The new time period of each output sample for the new transposed circuit is given by

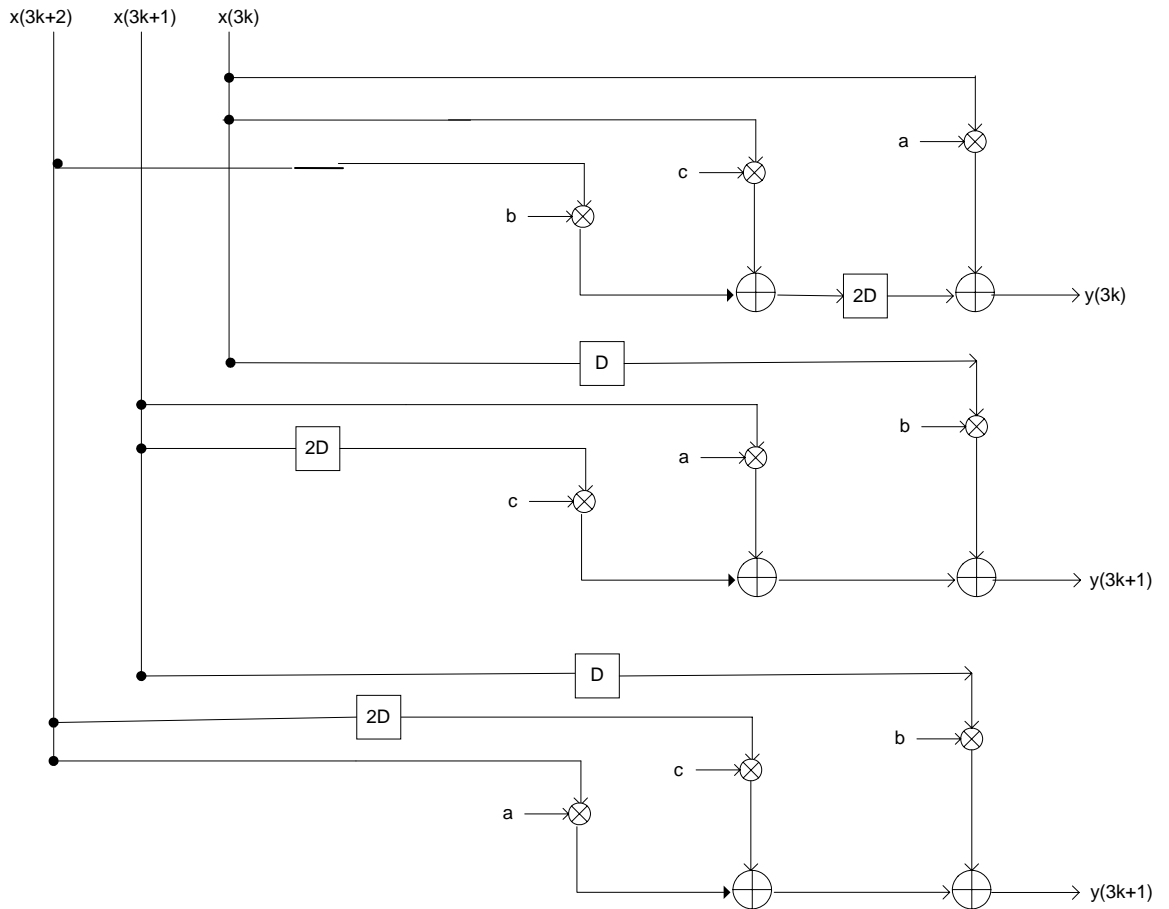
$$T_{\text{sample}} = T_m + T_a$$

7(b) . Block architecture for the circuit 6<sup>th</sup>-order FIR filter of block size of 3 using parallel processing is given by equations

$$y(3k) = ax(3k) + bx(3k-4) + cx(3k-6)$$

$$y(3k+1) = ax(3k+1) + bx(3k-3) + cx(3k-5)$$

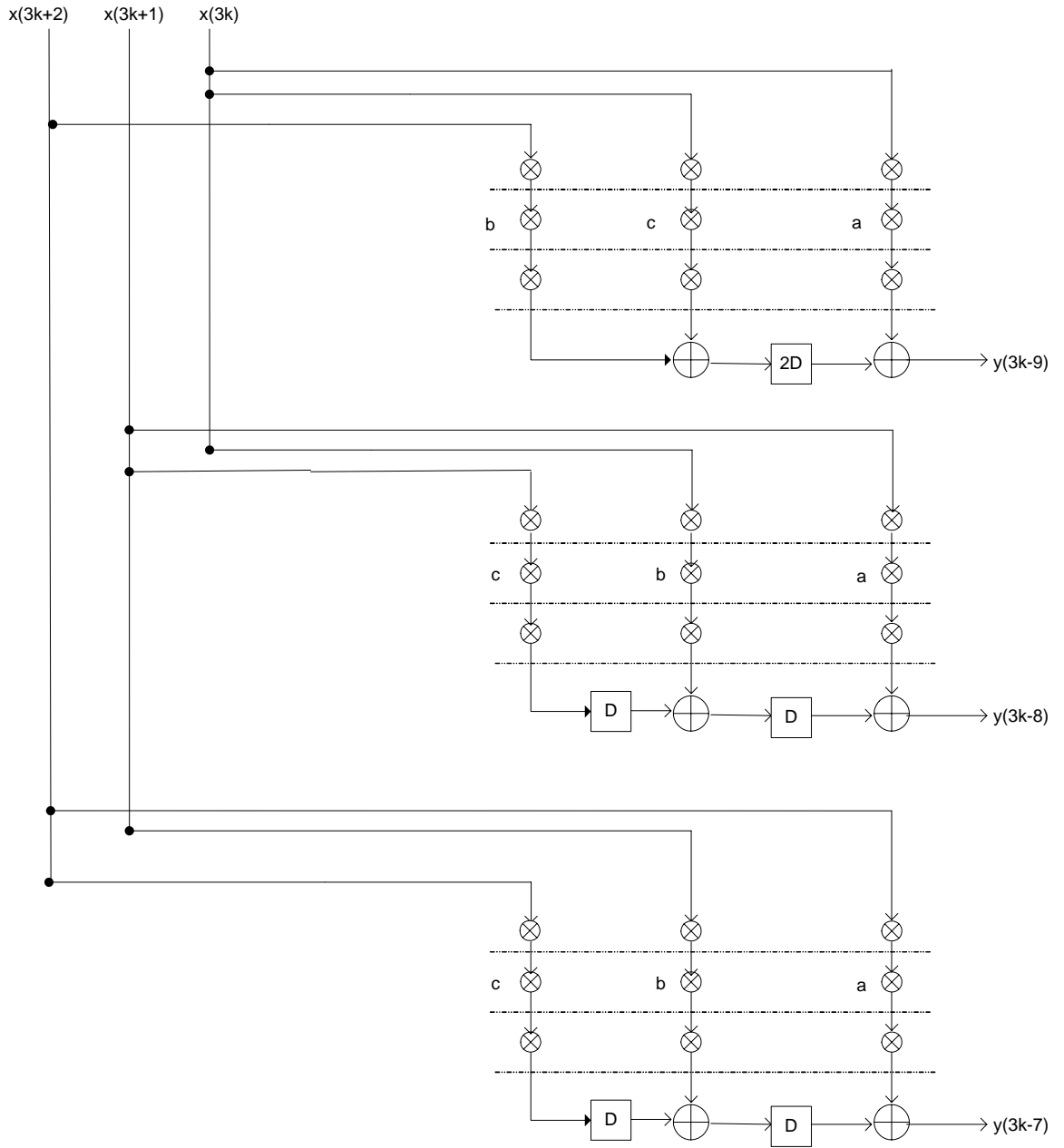
$$y(3k+2) = ax(3k+2) + bx(3k-2) + cx(3k-4)$$



Given that

$$T_m = 3T_a$$

Rearranging the pipelined parallel filter structure such that the clock period is one-fourth of a multiply-add time is given by

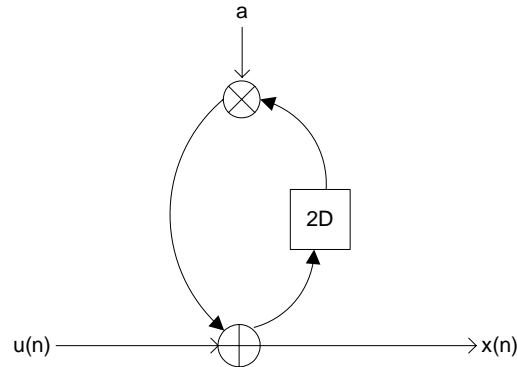


The above structure shows the pipelined parallel filter structure, in which the multiplier has been broken into three parts  $m_1$ ,  $m_2$  and  $m_3$ . Each part has the same computation time as addition computation. The pipelining latches are placed along the feed forward cutsets shown by dotted lines.

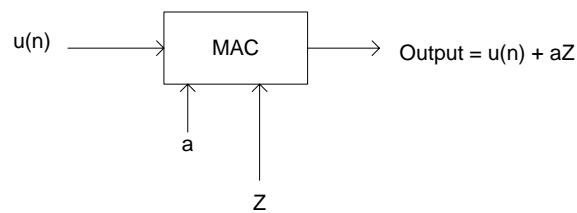
8(a). The given recursive filter is  

$$x(n) = ax(n-2) + u(n)$$

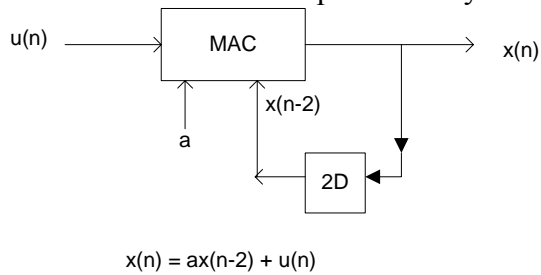
The circuit above is given by



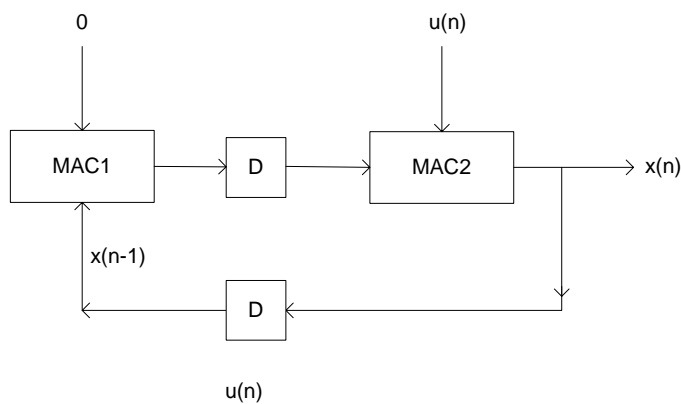
Breaking up the multiply-add operation into 2 components is done by using two Multiply Add Components (MAC) which is given by the figure



In our circuit MAC is represented by



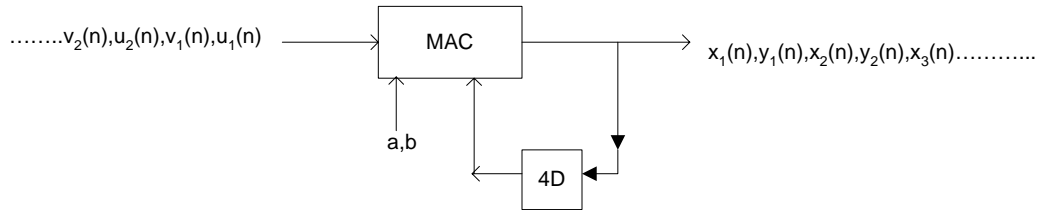
Redistributing the delay elements in the loop is given by



8(b). The given equation is

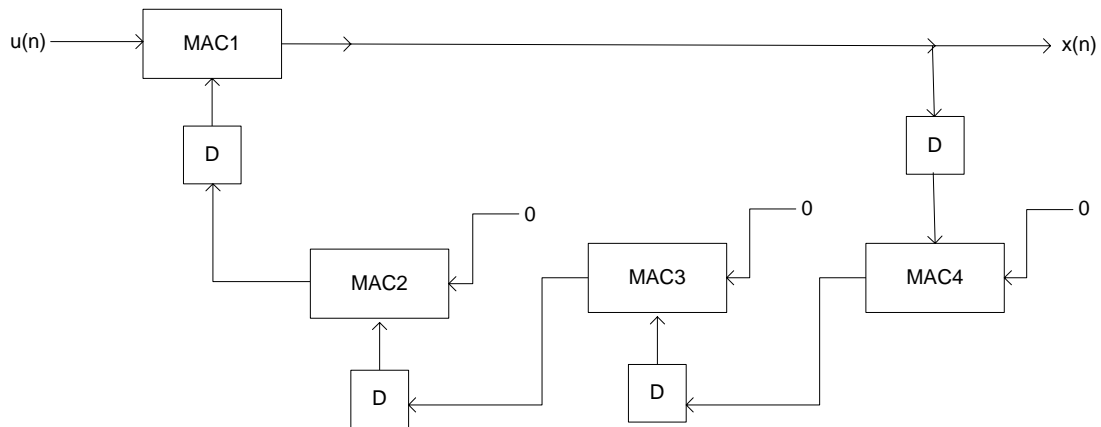
$$y(n) = by(n-2) + v(n)$$

First slow down the circuit by replacing the 2-delay with a 4-delay and then interleave the two computations. There appears an idle cycle in every two cycles. These idle cycles are used to operate  $v(n)$ .



Time	1	2	3	4	5	6	7	8	9	.....
Input	u1	v1	u2	v2	u3	v3	u4	v4	v5	.....
Output	x1	y1	x2	y2	x3	y3	x4	y4	x5	.....

Pipelining the multiply-add operation by 4 stages we get



9. Given that

Threshold voltage  $V_t = 0.4 \text{ V}$   
Initial Voltage supply  $V_o = 5 \text{ V}$

Let the level of pipelining be  $M$

Let  $\beta$  is the voltage reduction factor i.e. supply voltage can be reduced to  $\beta V_o$  for the pipelined system.

From (1) and (1a) we get  $\beta^2 \leq 1/5$   
 $\Rightarrow \beta = \sqrt{1/5} = 0.447$

Suppose that the pipelined system and the original system have the same sample rate, we have

$$M = \frac{\beta(V_o - V_t)^2}{(\beta V_o - V_t)^2}$$

Using the values of  $V_o$ ,  $V_t$  &  $\beta$  and solving for  $M$  we get

$$M = \left[ \frac{0.447(5 - 0.4)^2}{(0.447 * 5 - 0.4)^2} \right]$$

$$= \left[ 2.8 \right] = 3$$

Therefore, the system should be pipelined at 3 level. Substitute  $M=3$  into (3.9) and solve for  $\beta=0.427$ . The supply voltage for pipelined system is  $\beta V_o = 0.427 * 5 \text{ V} = 2.14 \text{ Volts}$ .

10. Given that

As required, filter (a) and filter (b) have equal clock period, therefore:

$$\frac{C_{\text{charge(a)}} V_a}{k(V_a - V_t)^2} = \frac{C_{\text{charge(b)}} V_b}{k(V_b - V_t)^2}$$

From the filter structure we know  $T_{\text{critical}} = 9T_a$  for filter (a),  $T_{\text{critical}} = 4T_a$  For filter(b),

$$\frac{C_{\text{charge(a)}}}{C_{\text{charge(b)}}} = \frac{\text{Propagation delay of circuit A}(T_{\text{critical(a)}})}{\text{Propagation delay of circuit B}(T_{\text{critical(b)}})} = \frac{V_b * (V_a - V_t)^2}{V_a * (V_b - V_t)^2}$$

Substitute the values of  $V_a = 4 \text{ V}$  and  $V_t = 0.5 \text{ V}$ , we have:

$$36(V_b)^2 - 85V_b + 9 = 0$$

$$V_{b1} = 2.25 \text{ Volt}$$

$$V_{b2} = 0.11 \text{ Volt} \text{-----discarded}$$

Compare to filter(a), the ratio of power saved by filter (b) is

$$1 - \frac{(V_b)^2}{(V_a)^2} = 1 - \frac{2.25^2}{4^2} = 68.34\%$$